Dr. ANANTHARAJ THALAIMALAI VANARAJ (Ph.D.)

Design Verification professional with 20 years' experience

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CONTACT

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EDUCATION

DOCTOR OF PHILOSOPHY • QUANTUM-DOT CELLULAR AUTOMATA (QCA)

MASTER OF TECHNOLOGY • VLSI SYSTEM

National Institute of Technology, Trichy, Tamilnadu, India

BACHELOR OF ENGINEERING • ELECTRONICS AND COMMUNICATION

Thanthai Periyar Government Institute of Technology (TPGIT), Madras University, Tamilnadu, India

KEY SKILLS

Verilog, System Verilog
System Verilog Assertions (SVA)
Universal Verification Methodology (UVM)
Formal Techniques
C++, Python

ONFI, PCIe, DDR, SAS, CXL

EDA Tools :Simulators, Debuggers, Emulation and Validation

Excellent communication
Responsible, Dynamic and Driven
Cross-Geo Project Execution
JIRA and EazyBI Dashboards
KPIs and QBRs

INNOVATION

Cross Functional Collaboration
Patents and Trade Secrets
Conferences and Publications

PROFILE

Data driven, result oriented leader with passion for functional verification and innovation infused execution.

EXPERIENCE

FORMAL VERIFICATION LEAD • AUG 2023 - PRESENT

Samsung Austin Semiconductors – Advanced Computing Lab

Formal Verification ownership for GPU RTL blocks; Mentoring members; JIRA driven task planning and resource estimation; Metrics based project reporting.

DIRECTOR/SENIOR TECHNOLOGIST • SEP 2008 – JULY 2023

Western Digital Technologies (SanDisk), Milpitas/Bangalore

Established Front End Design group for NAND Flash Memory development; Mentored team of 35+ engineers for RTL Design, Verification and Modeling; Developed and tracked KPIs for verification signoff; Handled verification closure using UVM and Formal Methodologies.

Deployed Zero Bug escape strategy across 10+ tape outs; Initiated System and Firmware level collaboration; Led JIRA/EazyBI dashboard reporting; Optimized verification regressions; Owned group level project planning, resource estimation and task scheduling for 2D/3D NAND Designs

VERIFICATION LEAD/SENIOR ENGINEER • JUL 2004 – AUG 2008

Wipro E-Peripherals, Samsung and LSI Logic India, Bangalore/Mysore

Played key role in System Verilog based verification of FPGA/ASIC designs for computer peripherals, wireless and storage controllers.

ACHIEVEMENTS

Established NAND Flash Design, Verification & Modeling Group (35+ team size) at Bangalore/Ofuna for project execution across US & APAC regions.

Improved Functional Verification efficiency up to 1.5x by leveraging Unified System Verilog Assertion Packages and shared SV-UVM Components.

Effected verification schedule reduction up to 20% between SanDisk and Kioxia by proposing unified SV-UVM Testbench Archiecture.

Deployed Left-Shift Strategy towards ~15% cost reduction by generalizing System FW Sequence Verification at Pre-Si & Post-Si Validation platforms.